IN THE CLAIMS

1-22. (Previously Canceled)

23. (Previously Added) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to at least one diode in the series of diodes for electrically bypassing at least one diode.

24. (Previously Added) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

25. (Previously Added) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one bypass transistor to plurality of diodes for electrically bypassing the plurality of diodes.

26. (Previously Added) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally off bypass transistor to at least one diode leaving the at least one diode unbypassed during normal operation and allowing the at least one diode to be selectively bypassed during testing operations.

27. (Previously Added) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally on bypass transistor to at least one diode leaving the at least one diode bypassed during normal operation and allowing the at least one diode to be selectively unbypassed during testing operations.

28. (Previously Added) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

29. (Previously Added) The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally off bypass transistor to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

30. (Previously Added) The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally on bypass transistor to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

31 (Previously Added) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

32. (Previously Added) The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally off bypass transistors to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

33. (Previously Added) The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally on bypass transistors to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

34. (Previously Added) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing at least one diode connected transistor.

35. (Previously Added) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one bypass transistor to plurality of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

36. (Previously Added) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally off bypass transistor to at least one diode connected transistor leaving the at least one diode connected transistor unbypassed during normal operation and allowing the at least one diode connected transistor to be selectively bypassed during testing operations.

37. (Previously Added) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally on bypass transistor to at least one diode connected transistor leaving the at least one diode

connected transistor bypassed during normal operation and allowing the at least one diode connected transistor to be selectively unbypassed during testing operations.

38. (Previously Added) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

39. (Previously Added) The method of claim 38 wherein coupling at least one bypass transistor to a plurality of diode connected transistors includes coupling a plurality of bypass transistors to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

40. (Previously Added) The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

41. (Previously Added) The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.

42. (Previously Added) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

43. (Previously Added) The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

44. (Previously Added) The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.

45. (Previously Added) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diodes in the series of diodes for electrically bypassing a portion of the plurality of diodes.

46. (Previously Added) The method of claim 45 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally off bypass transistor to a plurality of diodes leaving the portion of the plurality of diodes unbypassed during normal operation and allowing the portion of the plurality of diodes to be selectively bypassed during testing operations.

47. (Previously Added) The method of claim 45 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally on bypass transistor to a plurality of diodes leaving the portion of the plurality of diodes bypassed during normal operation and allowing the portion of the plurality of diodes to be selectively unbypassed during testing operations.